

Figure 1A: Computer Data Storage Architecture (Prior Art)

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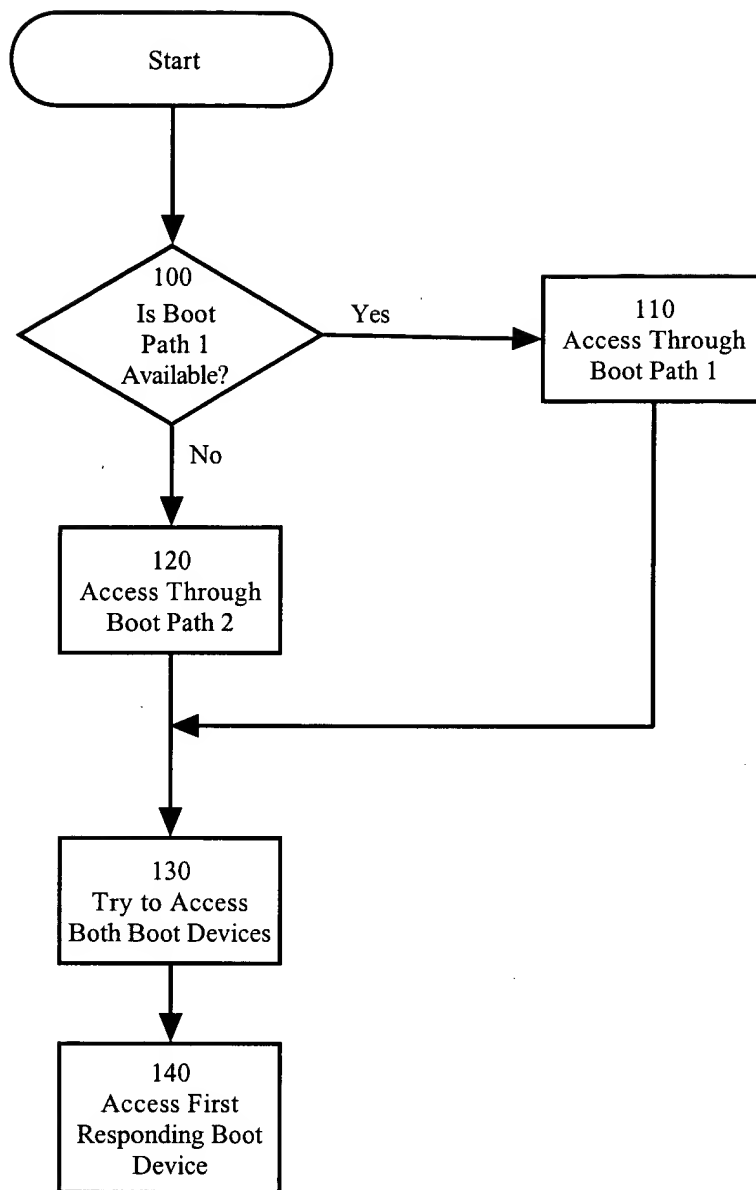


Figure 1B: Invention Data Access Process

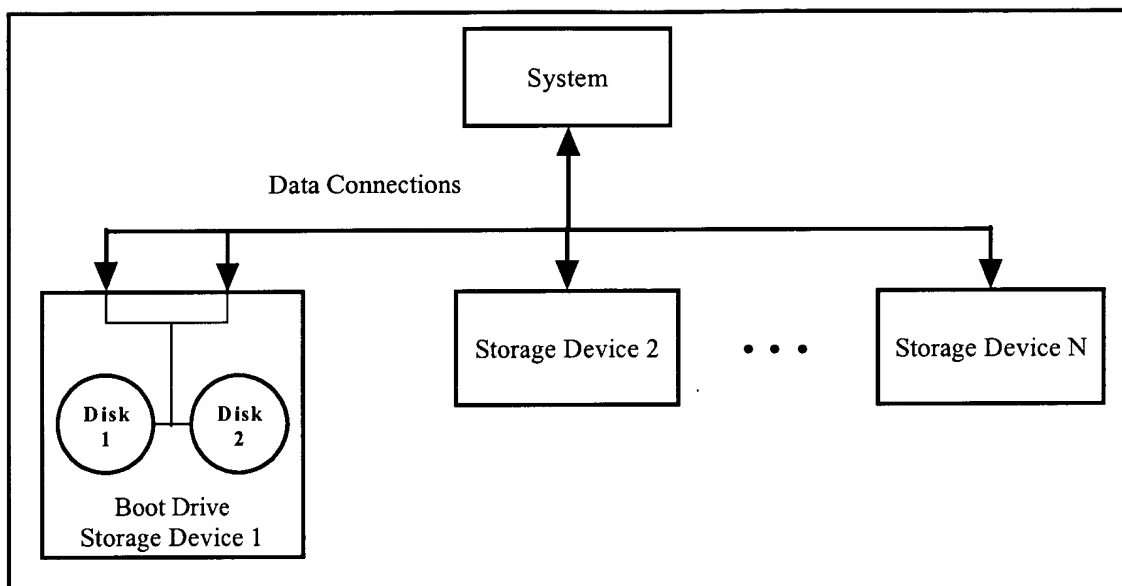


Figure 2: Computer Data Storage Architecture

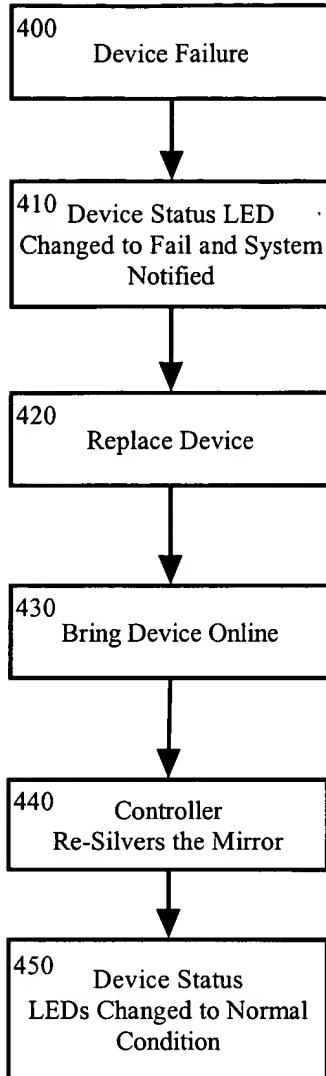


Figure 4: Invention Recovery from Failed Disk

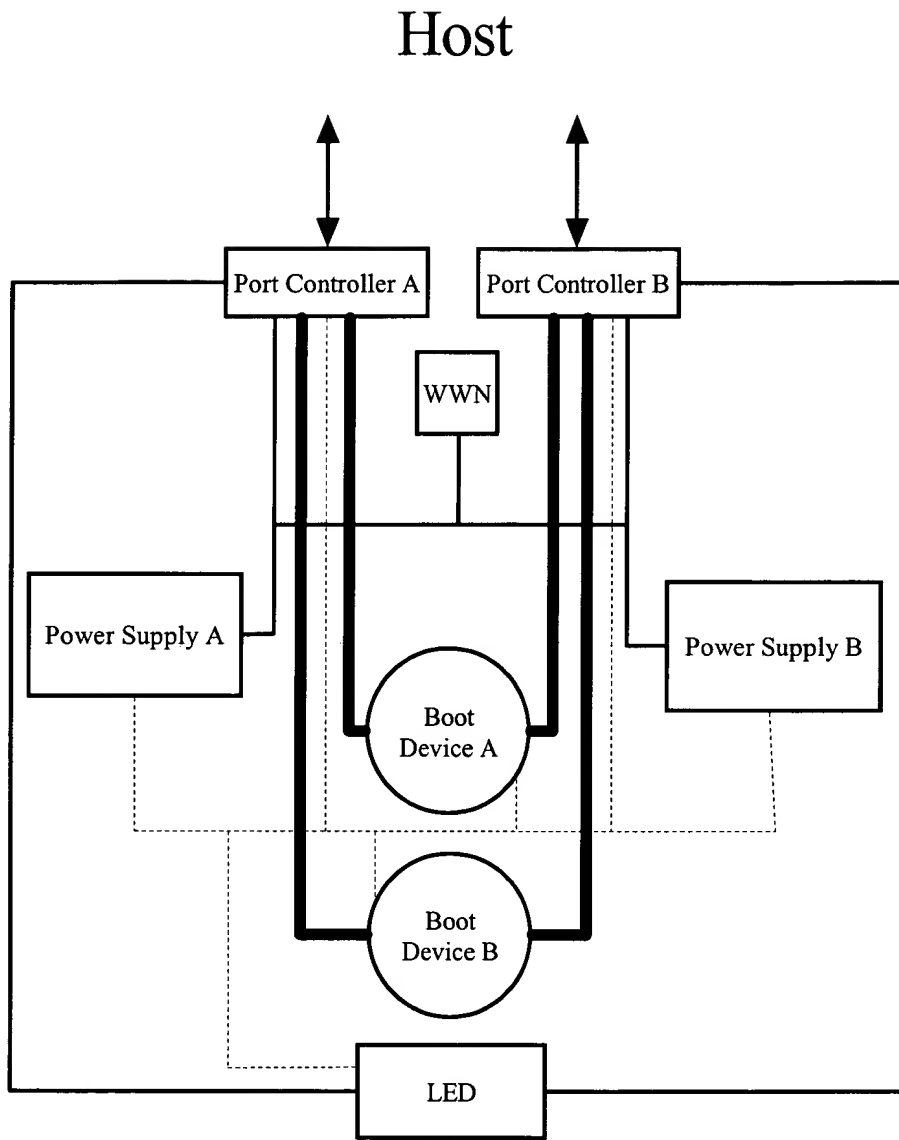


Figure 6: One Embodiment of the Present Invention

The diagram illustrates the system architecture with the following components and connections:

- 700 Host** is connected to **701 RS232**, **702 GBIC**, and **705 FRU-ID**.
- 701 RS232** is connected to **703 Serial**.
- 703 Serial**, **704 CPU MEM**, **706 Boot Flash**, **707 CPU**, **708 I2C**, and **709 RX TX REG** are connected to a central vertical bus.
- 702 GBIC** is connected to **710 QLogic**.
- 710 QLogic** is connected to **713 QLogic**.
- 713 QLogic** is connected to **714 BY PASS** and **715 BY PASS**.
- 714 BY PASS** and **715 BY PASS** are connected to **716 Frame Mid-Plane**.
- 705 FRU-ID** is connected to **711 Cache Controller**.
- 711 Cache Controller** is connected to **712 Staging Cache**.
- 712 Staging Cache** is connected to **711 Cache Controller**.
- 716 Frame Mid-Plane** is connected to **707 CPU**, **708 I2C**, **709 RX TX REG**, **714 BY PASS**, and **715 BY PASS**.
- 716 Frame Mid-Plane** has connections to **Power Supplies, WWN Unit and Other Controller**, **LED Unit**, and **Disk Drives**.

Figure 7: One Embodiment of a Port Controller